Tradeoffs And Optimization In Analog Cmos Design

This volume of The Circuits and Filters Handbook, Third Edition focuses on computer aided design and design automation. In the first part of the book, international contributors address topics such as the modeling of circuit performances, symbolic analysis methods, numerical analysis methods, design by optimization, statistical design optimization, and physical design automation. In the second half of the text, they turn their attention to RF CAD, high performance simulation, formal verification, RTK behavioral synthesis, system-level design, an Internet-based micro-electronic design automation framework, performance modeling, and embedded computing systems design.
This book (CCIS 839) constitutes the refereed proceedings of the First International Conference on Communication, Networks and Computings, CNC 2018, held in Gwalior, India, in March 2018. The 70 full papers were

carefully reviewed and selected from 182 submissions. The papers are organized in topical sections on wired and wireless communication systems, high dimensional data representation and processing, networks and information security, computing techniques for efficient networks design, electronic circuits for communication system.

Discover a fresh approach to efficient and insight-driven analog integrated circuit design in nanoscale-CMOS with this hands-on guide. Expert authors present a sizing methodology that employs SPICE-generated lookup tables, enabling close agreement between hand analysis and simulation. This enables the exploration of analog circuit tradeoffs using the gm/ID ratio as a central variable in script-based design flows, and eliminates time-consuming iterations in a circuit simulator. Supported by downloadable MATLAB code, and including over forty detailed worked examples, this book will provide professional analog circuit designers, researchers, and graduate students with the theoretical know-how and practical

*tools needed to acquire a systematic
and re-use oriented design style for
analog integrated circuits in modern
CMOS.*

*This book constitutes the thoroughly
refereed proceedings of the Third
International Conference on Advances in
Communication, Network, and Computing,
CNC 2012, held in Chennai, India,
February 24-25, 2012. The 41 revised
full papers presented together with 29
short papers and 14 poster papers were
carefully selected and reviewed from
425 submissions. The papers cover a
wide spectrum of issues in the field of
Information Technology, Networks,
Computational Engineering, Computer and
Telecommunication Technology, ranging
from theoretical and methodological
issues to advanced applications.*
*Computer Aided Design and Design
Automation*
Communication, Networks and Computing
Design and Analysis of Spiral Inductors
*Placement, Routing and Parasitic
Extraction Techniques*
The van der Pol Approach
*Ultra-low Voltage Low Power Active-RC
Filters and Amplifiers for Low Energy*

RF Receivers

In addition, the constrained optimization formulation of the analog design problem makes it easy for the user to study tradeoffs in the circuit design space by varying the performance constraints. Simulation results demonstrate the tool's ability to accurately synthesize high performance two-stage CMOS op amps in 2[mu]m and 1.2[mu]m CMOS processes."

Today's manufacturing systems are undergoing significant changes in the aspects of planning, production execution, and delivery. It is imperative to stay up-to-date on the latest trends in optimization to efficiently create products for the market. The Handbook of Research on Applied Optimization Methodologies in Manufacturing Systems is a pivotal reference source including the latest scholarly research on heuristic models for solving manufacturing and supply chain related problems. Featuring exhaustive coverage on a broad range of topics such as assembly ratio, car sequencing, and color constraints, this publication is ideally designed for practitioners seeking new comprehensive models for problem solving in manufacturing and supply chain management. This book introduces readers to a variety of tools for analog layout design automation. After discussing the placement and routing problem in electronic design automation (EDA), the authors overview a variety of automatic layout generation tools, as well as the most recent advances in analog layout-aware circuit sizing. The discussion includes different methods for automatic placement (a template-based Placer and an optimization-based Placer), a fully-automatic Router and an empirical-based Parasitic Extractor. The concepts and algorithms of all the modules are thoroughly described, enabling readers to reproduce the methodologies, improve the quality of their designs, or use them as starting point for a

new tool. All the methods described are applied to practical examples for a 130nm design process, as well as placement and routing benchmark sets.

This book gathers selected research papers presented at the Second International Conference on Energy Systems, Drives and Automations (ESDA 2019), held in Kolkata on 28–29 December 2019. It covers a broad range of topics in the fields of renewable energy, power management, drive systems for electrical machines and automation. Also discussing a variety of related tools and techniques, the book offers a valuable resource for researchers, professionals and students in electrical and mechanical engineering disciplines.
Tradeoffs and Optimization in Analog CMOS Design
Circuit Design, Layout, and Simulation

Advances in Communication, Network, and Computing
Electronic Design Automation of Analog ICs combining Gradient Models with Multi-Objective Evolutionary Algorithms
Automating Analog Circuit Design Using Constrained Optimization Techniques
CMOS: Front-End Electronics for Radiation Sensors offers a comprehensive introduction to integrated front-end electronics for radiation detectors, focusing on devices that capture individual particles or photons and are used in nuclear and high energy physics, space instrumentation, medical physics, homeland security, and related fields. Emphasizing practical design and implementation, this book: Covers the

*fundamental principles of signal
processing for radiation detectors
Discusses the relevant analog building
blocks used in the front-end
electronics Employs systematically weak
and moderate inversion regimes in
circuit analysis Makes complex topics
such as noise and circuit-weighting
functions more accessible Includes
numerical examples where appropriate
CMOS: Front-End Electronics for
Radiation Sensors provides specialized
knowledge previously obtained only
through the study of multiple technical
and scientific papers. It is an ideal
text for students of physics and
electronics engineering, as well as a
useful reference for experienced
practitioners.*

*In response to a request from the
Defense Advanced Research Projects
Agency, the committee studied a range
of issues to help identify what
strategies the Department of Defense
might follow to meet its need for
flexible, rapidly deployable
communications systems. Taking into
account the military's particular
requirements for security,*

interoperability, and other capabilities as well as the extent to which commercial technology development can be expected to support these and related needs, the book recommends systems and component research as well as organizational changes to help the DOD field state-of-the-art, cost-effective untethered communications systems. In addition to advising DARPA on where its investment in information technology for mobile wireless communications systems can have the greatest impact, the book explores the evolution of wireless technology, the often fruitful synergy between commercial and military research and development efforts, and the technical challenges still to be overcome in making the dream of "anytime, anywhere" communications a reality.
In addition, the constrained optimization formulation of the analog design problem makes it easy for the user to study tradeoffs in the circuit design space by varying the performance constraints. Simulation results demonstrate the tool's ability to accurately synthesize high performance

two-stage CMOS op amps in 2[mu]m and 1.2 [mu]m CMOS processes."
This book introduces readers to a variety of tools for automatic analog integrated circuit (IC) sizing and optimization. The authors provide a historical perspective on the early methods proposed to tackle automatic analog circuit sizing, with emphasis on the methodologies to size and optimize the circuit, and on the methodologies to estimate the circuit's performance. The discussion also includes robust circuit design and optimization and the most recent advances in layout-aware analog sizing approaches. The authors describe a methodology for an automatic flow for analog IC design, including details of the inputs and interfaces, multi-objective optimization techniques, and the enhancements made in the base implementation by using machine leaning techniques. The Gradient model is discussed in detail, along with the methods to include layout effects in the circuit sizing. The concepts and algorithms of all the modules are thoroughly described, enabling readers to reproduce the

methodologies, improve the quality of their designs, or use them as starting point for a new tool. An extensive set of application examples is included to demonstrate the capabilities and features of the methodologies described.

Integrated Circuits/Microchips

Handbook of Research on Applied Optimization Methodologies in Manufacturing Systems

System Perspectives and Design Aspects

The Evolution of Untethered Communications

Charge-Sharing SAR ADCs for Low-Voltage Low-Power Applications

CMOS

Analog CMOS integrated circuits are in widespread use for communications, entertainment, multimedia, biomedical, and many other applications that interface with the physical world. Although analog CMOS design is greatly complicated by the design choices of drain current, channel width, and channel length present for every MOS device in a circuit, these design choices afford significant opportunities for optimizing circuit performance. This book addresses tradeoffs and optimization of device and circuit performance for selections of the

drain current, inversion coefficient, and channel length, where channel width is implicitly considered. The inversion coefficient is used as a technology independent measure of MOS inversion that permits design freely in weak, moderate, and strong inversion. This book details the significant performance tradeoffs available in analog CMOS design and guides the designer towards optimum design by describing: An interpretation of MOS modeling for the analog designer, motivated by the EKV MOS model, using tabulated hand expressions and figures that give performance and tradeoffs for the design choices of drain current, inversion coefficient, and channel length; performance includes effective gate-source bias and drain-source saturation voltages, transconductance efficiency, transconductance distortion, normalized drain-source conductance, capacitances, gain and bandwidth measures, thermal and flicker noise, mismatch, and gate and drain leakage current Measured data that validates the inclusion of important small-geometry effects like velocity saturation, vertical-field mobility reduction, drain-induced barrier lowering, and inversion-level increases in gate-referred, flicker noise voltage In-depth treatment of moderate inversion, which offers low bias compliance voltages, high transconductance

efficiency, and good immunity to velocity saturation effects for circuits designed in modern, low-voltage processes Fabricated design examples that include operational transconductance amplifiers optimized for various tradeoffs in DC and AC performance, and micropower, low-noise preamplifiers optimized for minimum thermal and flicker noise A design spreadsheet, available at the book web site, that facilitates rapid, optimum design of MOS devices and circuits Tradeoffs and Optimization in Analog CMOS Design is the first book dedicated to this important topic. It will help practicing analog circuit designers and advanced students of electrical engineering build design intuition, rapidly optimize circuit performance during initial design, and minimize trial-and-error circuit simulations.

A thoroughly updated third edition of an classic text, perfect for practical transistor design and in the classroom. It includes a variety of recent developments, reorganized chapters, and additional end-of-chapter homework exercises, making it ideal for senior undergraduate and graduate students taking advanced semiconductor devices courses.

It is a great honor to provide a few words of introduction for Dr. Georges Gielen's and Prof. Willy Sansen's book "Symbolic analysis for

*automated design of analog integrated circuits".
The symbolic analysis method presented in this
book represents a significant step forward in the
area of analog circuit design. As demonstrated in
this book, symbolic analysis opens up new
possibilities for the development of computer-
aided design (CAD) tools that can analyze an
analog circuit topology and automatically size
the components for a given set of specifications.
Symbolic analysis even has the potential to
improve the training of young analog circuit
designers and to guide more experienced
designers through second-order phenomena
such as distortion. This book can also serve as
an excellent reference for researchers in the
analog circuit design area and creators of CAD
tools, as it provides a comprehensive overview
and comparison of various approaches for
analog circuit design automation and an
extensive bibliography. The world is essentially
analog in nature, hence most electronic systems
involve both analog and digital circuitry. As the
number of transistors that can be integrated on a
single integrated circuit (IC) substrate steadily
increases over time, an ever increasing number
of systems will be implemented with one, or a
few, very complex ICs because of their lower
production costs.
This book introduces readers to the potential of*

charge-sharing (CS) successive approximation register (SAR) analog-to-digital converters (ADCs), while providing extensive analysis of the factors that limit the performance of the CS topology. The authors present guidelines and useful techniques for mitigating the limitations of the architecture, while focusing on the implementation under restricted power budgets and voltage supplies.

Design of Analog CMOS Integrated Circuits

模拟CMOS集成电路设计(——())

The Designer's Companion

FM-UWB Transceivers for Autonomous Wireless Systems

Energy Systems, Drives and Automations

Power-Efficient High-Speed Parallel-Sampling ADCs for Broadband Multi-carrier Systems

This book applies to the scientific area of electronic design automation (EDA) and addresses the automatic sizing of analog integrated circuits (ICs). Particularly, this book presents an approach to enhance a state-of-the-art layout-aware circuit-level optimizer (GENOM-POF), by embedding statistical knowledge from an automatically generated gradient model into the multi-objective multi-constraint optimization kernel based on the NSGA-II algorithm. The results showed allow the designer to explore the different trade-offs of the solution space, both through the achieved device sizes, or the respective layout solutions.

Modern transceiver systems require diversified design aspects as various radio and sensor applications have emerged. Choosing the right architecture and understanding interference and linearity issues are important for multi-standard cellular transceivers and software-defined radios. A millimeter-wave complementary metal–oxide–semiconductor (CMOS) transceiver design for multi-Gb/s data transmission is another challenging area. Energy-efficient short-range radios for body area networks and sensor networks have recently received great attention. To meet different design requirements, gaining good system perspectives is important. Wireless Transceiver Circuits: System Perspectives and Design Aspects offers an in-depth look at integrated circuit (IC) design for modern transceiver circuits and wireless systems. Ranging in scope from system perspectives to practical circuit design for emerging wireless applications, this cutting-edge book: Provides system design considerations in modern transceiver design Covers both systems and circuits for the millimeter-wave transceiver design Introduces four energy-efficient short-range radios for biomedical and wireless connectivity applications Emphasizes key building blocks in modern transceivers and transmitters, including frequency synthesizers and digital-intensive phase modulators Featuring contributions from renowned international experts in industry and academia, Wireless Transceiver Circuits: System Perspectives and Design Aspects makes an ideal reference for engineers and researchers in the

area of wireless systems and circuits.

This book presents a tutorial review of van der Pol model, a universal oscillator model for the analysis of modern RC−oscillators in weak and strong nonlinear regimes. A detailed analysis of the injection locking in van der Pol oscillators is also presented. The relation between the van der Pol parameters and several circuit implementations in CMOS nanotechnology is given, showing that this theory is very useful in the optimization of oscillator key parameters, such as: frequency, amplitude and phase relationship. The authors discuss three different examples: active coupling RC−oscillators, capacitive coupling RC−oscillators, and two-integrator oscillator working in the sinusoidal regime. · Provides a detailed tutorial on the van der Pol oscillator model, which can be the basis for the analysis of modern RC−oscillators in weak and strong nonlinear regimes; · Demonstrations the relationship between the van der Pol parameters and several circuit implementations in CMOS nanotechnology, showing that this theory is a powerful tool in the optimization of key oscillator parameters; · Provides three circuit prototypes implemented in modern CMOS nanotechnology in the GHz range, with applications in low area, low power, low cost, wireless sensor network (WSN) applications (e.g. IoT, BLE). TodayOCOs professionals are constantly striving to create sensor technology and systems with lower cost and higher efficiency. Miniaturization and standardization have become critical drivers for cost reduction in the design and development process,

giving rise to a new era of smart sensors and actuators. These devices contain more components, but normally provide significant cost savings due to wider applicability and mass production. This first-of-its-kind resource presents methods for cost optimization of smart microsystems to help you select highly cost-efficient implementation variants. Written by leading experts, the book offers detailed coverage of the key topics that you need to understand for your work in the field, such as methods for cost estimation, holistic design optimization, a methodology for a cost-driven design, and applied cost optimization. This practical book focuses on fundamental cost influences rather than absolute numbers, helping you appreciate relative values which reflect the competitive advantage of the various design implementations. Moreover, you find specific recommendations on which cost-reduction methods will be most advantageous in varying situations. This forward-looking volume provides keen insight into the underlying factors which drive the current economics and determine future trends of smart microsystems.
Using Pre-Computed Lookup Tables
Analog Integrated Circuit Design Automation
Third International Conference, CNC 2012, Chennai, India, February 24-25, 2012, Revised Selected Papers
Trade-Offs in Analog Circuit Design
Quadrature RC−Oscillators
Proceedings of ESDA 2019
The book addresses the critical challenges faced by the ever-expanding wireless communication market and the

*increasing frequency of operation due to continuous
innovation of high performance integrated passive devices.
The challenges like low quality factor, design complexity,
manufacturability, processing cost, etc., are studied with
examples and specifics. Silicon on-chip inductor was first
reported in 1990 by Nguyen and Meyer in a 0.8 μm silicon
bipolar complementary metal oxide semiconductor
technology (BiCMOS). Since then, there has been an
enormous progress in the research on the performance
trends, design and optimization, modeling, quality factor
enhancement techniques, etc., of spiral inductors and
significant results are reported in literature for various
applications. This book introduces an efficient method of
determining the optimized layout of on chip spiral inductor.
The important fundamental tradeoffs of the design like
quality factor and area, quality factor and inductance,
quality factor and operating frequency, maximum quality
factor and the peak frequency is also explored. The authors
proposed an algorithm for accurate design and optimization
of spiral inductors using a 3D electromagnetic simulator
with minimum number of inductor structure simulations and
thereby reducing its long computation time. A new multilayer
pyramidal symmetric inductor structure is also proposed in
this book. Being multilevel, the proposed inductor achieves
high inductance to area ratio and hence occupies smaller
silicon area.
Praise for CMOS: Circuit Design, Layout, and
SimulationRevised Second Edition from the Technical
Reviewers "A refreshing industrial flavor. Design concepts*

are presented as they are needed for 'just-in-time' learning. Simulating and designing circuits using SPICE is emphasized with literally hundreds of examples. Very few textbooks contain as much detail as this one. Highly recommended!" --Paul M. Furth, New Mexico State University "This book builds a solid knowledge of CMOS circuit design from the ground up. With coverage of process integration, layout, analog and digital models, noise mechanisms, memory circuits, references, amplifiers, PLLs/DLLs, dynamic circuits, and data converters, the text is an excellent reference for both experienced and novice designers alike." --Tyler J. Gomm, Design Engineer, Micron Technology, Inc. "The Second Edition builds upon the success of the first with new chapters that cover additional material such as oversampled converters and non-volatile memories. This is becoming the de facto standard textbook to have on every analog and mixed-signal designer's bookshelf." --Joe Walsh, Design Engineer, AMI Semiconductor CMOS circuits from design to implementation CMOS: Circuit Design, Layout, and Simulation, Revised Second Edition covers the practical design of both analog and digital integrated circuits, offering a vital, contemporary view of a wide range of analog/digital circuit blocks, the BSIM model, data converter architectures, and much more. This edition takes a two-path approach to the topics: design techniques are developed for both long- and short-channel CMOS technologies and then compared. The results are multidimensional explanations that allow readers to gain deep insight into the design process. Features include: Updated materials to reflect

CMOS technology's movement into nanometer sizes Discussions on phase- and delay-locked loops, mixed-signal circuits, data converters, and circuit noise More than 1,000 figures, 200 examples, and over 500 end-of-chapter problems In-depth coverage of both analog and digital circuit-level design techniques Real-world process parameters and design rules The book's Web site, CMOSedu.com, provides: solutions to the book's problems; additional homework problems without solutions; SPICE simulation examples using HSPICE, LTspice, and WinSpice; layout tools and examples for actually fabricating a chip; and videos to aid learning

**

CMOS

MOS.

This book comprises select proceedings of the International Conference on VLSI, Communication and Signal processing (VCAS 2020). The contents are broadly divided into three topics – VLSI, Communication, and Signal Processing. The book focuses on the latest innovations, trends, and challenges encountered in the different areas of electronics and communication, especially in the area of microelectronics and VLSI design, communication systems and networks, and image and signal processing. It also offers potential solutions and provides an insight into various emerging areas such as Internet of Things (IoT), System on a Chip (SoC), Sensor Networks, underwater and underground communication networks etc. This book will be useful for academicians and professionals alike.

Sizing of Cell-level Analog Circuits Using Constrained Optimization Techniques
Optimization for Machine Learning
Knowledge-Based Intelligent Information and Engineering Systems
Cost-Driven Design of Smart Microsystems
Accurate Analog Synthesis with Circuit Matrix Models
Fundamentals of Modern VLSI Devices
Improving the performance of existing technologies has always been a focal practice in the development of computational systems. However, as circuitry is becoming more complex, conventional techniques are becoming outdated and new research methodologies are being implemented by designers. Performance Optimization Techniques in Analog, Mix-Signal, and Radio-Frequency Circuit Design features recent advances in the engineering of integrated systems with prominence placed on methods for maximizing the functionality of these systems. This book emphasizes prospective trends in the field and is an essential reference source for researchers, practitioners, engineers, and technology designers interested in emerging research and techniques in the performance optimization of different circuit designs. Embedded systems are nearly ubiquitous, and

books on individual topics or components of embedded systems are equally abundant. Unfortunately, for those designers who thirst for knowledge of the big picture of embedded systems there is not a drop to drink. Until now. The Embedded Systems Handbook is an oasis of information, offering a mix of basic a As the frequency of communication systems increases and the dimensions of transistors are reduced, more and more stringent performance requirements are placed on analog circuits. This is a trend that is bound to continue for the foreseeable future and while it does, understanding performance trade-offs will constitute a vital part of the analog design process. It is the insight and intuition obtained from a fundamental understanding of performance conflicts and trade-offs, that ultimately provides the designer with the basic tools necessary for effective and creative analog design. Trade-offs in Analog Circuit Design, which is devoted to the understanding of trade-offs in analog design, is quite unique in that it draws together fundamental material from, and identifies interrelationships within, a number of key analog circuits. The book covers ten subject areas: Design methodology, Technology, General Performance, Filters, Switched

Circuits, Oscillators, Data Converters, Transceivers, Neural Processing, and Analog CAD. Within these subject areas it deals with a wide diversity of trade-offs ranging from frequency-dynamic range and power, gain-bandwidth, speed-dynamic range and phase noise, to tradeoffs in design for manufacture and IC layout. The book has by far transcended its original scope and has become both a designer's companion as well as a graduate textbook. An important feature of this book is that it promotes an intuitive approach to understanding analog circuits by explaining fundamental relationships and, in many cases, providing practical illustrative examples to demonstrate the inherent basic interrelationships and trade-offs. Trade-offs in Analog Circuit Design draws together 34 contributions from some of the world's most eminent analog circuits-and-systems designers to provide, for the first time, a comprehensive text devoted to a very important and timely approach to analog circuit design.

An up-to-date account of the interplay between optimization and machine learning, accessible to students and researchers in both communities. The interplay between optimization and machine learning is one of

the most important developments in modern computational science. Optimization formulations and methods are proving to be vital in designing algorithms to extract essential knowledge from huge volumes of data. Machine learning, however, is not simply a consumer of optimization technology but a rapidly evolving field that is itself generating new optimization ideas. This book captures the state of the art of the interaction between optimization and machine learning in a way that is accessible to researchers in both fields. Optimization approaches have enjoyed prominence in machine learning because of their wide applicability and attractive theoretical properties. The increasing complexity, size, and variety of today's machine learning models call for the reassessment of existing assumptions. This book starts the process of reassessment. It describes the resurgence in novel contexts of established frameworks such as first-order methods, stochastic approximations, convex relaxations, interior-point methods, and proximal methods. It also devotes attention to newer themes such as regularized optimization, robust optimization, gradient and subgradient methods, splitting techniques, and second-order methods. Many

of these techniques draw inspiration from other fields, including operations research, theoretical computer science, and subfields of optimization. The book will enrich the ongoing cross-fertilization between the machine learning community and these other fields, and within the broader optimization community.

First International Conference, CNC 2018, Gwalior, India, March 22-24, 2018, Revised Selected Papers

Symbolic Analysis for Automated Design of Analog Integrated Circuits

Embedded Systems Handbook

Recent Trends in Electronics and Communication

Feedback Linearization of RF Power Amplifiers

Noise, Speed, and Power Tradeoffs in Pipelined Analog to Digital Converters

Improving the performance of the power amplifier is the most pressing problem facing designers of modern radio-frequency (RF) transceivers. Linearity and power efficiency of the transmit path are of utmost importance, and the power amplifier has proven to be the bottleneck for both. High linearity enables transmission at the highest data rates for a given channel bandwidth, and power efficiency prolongs battery lifetime in portable units and reduces heat dissipation

in high-power transmitters. Cartesian feedback is a power amplifier linearization technique that acts to soften the tradeoff between power efficiency and linearity in power amplifiers. Despite its compelling, fundamental advantages, the technique has not enjoyed widespread acceptance because of certain implementation difficulties. Feedback Linearization of RF Power Amplifiers introduces new techniques for overcoming the challenges faced by the designer of a Cartesian feedback system. The theory of the new techniques are described and analyzed in detail. The book culminates with the results of the first known fully integrated Cartesian feedback power amplifier system, whose design was enabled by the techniques described. Feedback Linearization of RF Power Amplifiers is a valuable reference work for engineers in the telecommunications industry, industry researchers, academic researchers. This book constitutes the refereed proceedings of the 4th IFIP WG 5.5/SOCOLNET Doctoral Conference on Computing, Electrical and Industrial Systems, DoCEIS 2013, held in Costa de Caparica, Portugal, in April 2013. The 69 revised full papers were carefully reviewed and selected from numerous submissions. They cover a wide spectrum of topics ranging from collaborative enterprise networks to microelectronics. The papers are organized in the following topical sections: collaborative enterprise networks; service orientation; intelligent computational

systems; computational systems; computational systems applications; perceptional systems; robotics and manufacturing; embedded systems and Petri nets; control and decision; integration of power electronics systems with ICT; energy generation; energy distribution; energy transformation; optimization techniques in energy; telecommunications; electronics: devices design; electronics: amplifiers; electronics: RF applications; and electronics: applications.

Significant research effort has been devoted to the study and realization of autonomous wireless systems for wireless sensor and personal-area networking, the internet of things, and machine-to-machine communications. Low-power RF integrated circuits, an energy harvester and a power management circuit are fundamental elements of these systems. An FM-UWB Transceiver for Autonomous Wireless Systems presents state-of-the-art developments in low-power FM-UWB transceiver realizations. The design, performance and implementation of prototype transceivers in CMOS technology are presented. A working hardware realization of an autonomous node that includes a prototype power management circuit is also proposed and detailed in this book. Technical topics include: Low-complexity FM-UWB modulation schemesLow-power FM-UWB transceiver prototypes in CMOS technologyCMOS on-chip digital calibration techniquesSolar power harvester and power management in CMOS for

low-power RF circuits An FM-UWB Transceiver for Autonomous Wireless Systems is an ideal text and reference for engineers working in wireless communication industries, as well as academic staff and graduate students engaged in electrical engineering and communication systems research.

Analog Optical Links presents the basis for the design of analog links. Following an introductory chapter, there is a chapter devoted to the development of the small signal models for common electro-optical components used in both direct and external modulation. However this is not a device book, so the theory of their operation is discussed only insofar as it is helpful in understanding the small signal models that result. These device models are then combined to form a complete link. With these analytical tools in place, a chapter is devoted to examining in detail each of the four primary link parameters; gain, bandwidth, noise figure and dynamic range. Of particular interest is the inter-relation between device and link parameters. A final chapter explores some of the trade offs among the primary link parameters.

Select Proceedings of VCAS 2020

Theory and Practice

Analog Optical Links

4th IFIP WG 5.5/SOCOLNET Doctoral Conference on Computing, Electrical and Industrial Systems, DoCEIS 2013, Costa de Caparica, Portugal, April 15-17, 2013, Proceedings

Wireless Transceiver Circuits
Front-End Electronics for Radiation Sensors
This book addresses the challenges of designing high
performance analog-to-digital converters (ADCs) based
on the "smart data converters" concept, which implies
context awareness, on-chip intelligence and adaptation.
Readers will learn to exploit various information either
a-priori or a-posteriori (obtained from devices, signals,
applications or the ambient situations, etc.) for circuit
and architecture optimization during the design phase
or adaptation during operation, to enhance data
converters performance, flexibility, robustness and
power-efficiency. The authors focus on exploiting the a-
priori knowledge of the system/application to develop
enhancement techniques for ADCs, with particular
emphasis on improving the power efficiency of high-
speed and high-resolution ADCs for broadband multi-
carrier systems.
Automated synthesis is imperative for the rapid design
of analog circuits. Knowledge based and optimization
based methods have emerged to provide solutions for
analog synthesis, especially for device sizing. Posing
analog sizing as a constrained optimization problem
facilitates the application of many well developed
algorithms for this purpose. All optimization based
sizing methods are based on the common thread of
design space exploration and performance evaluation.
In this dissertation we develop methods using Circuit
Matrix Models to estimate the performance of analog
circuits. Using these models the entire a.c. behavior of
the circuit is captured. With the use of matrix models,
the limitation that a circuit can by synthesized for the
modeled performance specifications is eliminated. Any
linear performance characteristic can be calculated

from the models. Analog circuits need to be designed with high accuracy. With circuit matrix models it is seen that performance prediction is precise and synthesized circuits are very accurate. We then develop techniques to expedite synthesis by making matrix model evaluation extremely fast. The first technique uses hashing for obtaining the desired speedup. This technique takes advantage of matrix elements being dependent on a subset of design variables. Design sub-spaces are visited several times when the entire space is being explored in a synthesis run. Hash tables save the matrix element values computed in the visited subspace and reuse them when that subspace is visited again. The second technique has a nearest neighbor searching algorithm at its core. It uses values at design points visited to incrementally compute values at neighboring design points. A first order Taylor series approximation is sufficient for such incremental computation and this makes performance estimation procedure extremely fast. A balanced box decomposition tree data structure makes detecting exact or approximate neighbors quite efficient. Using this method, very few computations are required during the synthesis process. These methods impart more than 10x speedup to the synthesis process. Layout parasitics are detrimental to the performance of analog circuits. Considering their effects early in the design flow is essential for achieving designs with parasitic closure. We have developed circuit matrix models inclusive of parasitic effects. The models use area and perimeter as predictor variables and can be used to compute parasitic inclusive matrix element values for many geometries. Thus, the most suitable geometry for component modules is selected dynamically by the

optimizer as a part of synthesis. Operational amplifiers and filter topologies have been synthesized by this method as a part of this work. The optimization objectives for analog circuits can be conflicting and often for improving a particular performance several others have to be sacrificed. Considering the performance tradeoffs is quite important for such multi-objective optimization problems. The developed circuit matrix models have been used to generate parasitic-aware Pareto-optimal performance curves. The method stores an archive of non-dominated performance points and the corresponding design points that achieve this performance. This can be used for determining the limits of achievable performance for a given topology as well as for sizing.

Delegates and friends, we are very pleased to extend to you a warm welcome to this, the 12th International Conference on Knowledge-Based and Intelligent Information and Engineering Systems organised by the Faculty of Electrical Engineering and Computing at the University of Zagreb, in association with KES International. For over a decade, KES International has provided an annual wide-spectrum intelligent systems conference for the applied arti?cial intelligence researchc- munity. Having originated in Australia and been held there during 1997–99,the conference visited the UK in 2000,Japan in 2001, Italy in 2002,the UK in 2003, New Zealand in 2004, Australia in 2005, the UK in 2006, Italy in 2007, and now in Zagreb, Croatia in 2008. It is planned that KES 2009 will be held in Santiago, Chile before returning to the UK in 2010. The KES conference is - ture and regularlyattracts severalhundred delegates. As it encompassesa broad range of intelligent systems topics, it provides

delegates with an opportunity to mix with researchers from other groups and learn from them. The conference is linked to the InternationalJournalof Intelligent and Knowledge-BasedSystems, published by IOS Press under KES editorship. Extended and enhanced versions of the best papers presented at the KES conference may be published in the Journal. In addition to the annual wide-range intelligent systems conference,KES has run successful symposia in several speci?c areas of the discipline. Agents and Multi-Agent Systems is a popular area of research.
Automatic Analog IC Sizing and Optimization Constrained with PVT Corners and Layout Effects
Performance Optimization Techniques in Analog, Mixed-Signal, and Radio-Frequency Circuit Design
Selected Papers on Computer-aided Design of Analog Networks
Systematic Design of Analog CMOS Circuits
12th International Conference, KES 2008, Zagreb, Croatia, September 3-5, 2008, Proceedings
Technological Innovation for the Internet of Things